*Patent*

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**
**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re Application of:

Cynthia Bertini, et al. Group Art Unit: 2128

Serial Number: 10/065,801 Examiner: Patel, Shambhavi K.

Filed: 11/20/2002

For: METHOD AND SYSTEM FOR MANAGING ELECTRICAL SCHEMATIC DATA

Attorney Docket No: 81045450 (FGT 2358 ROA)

**CERTIFICATE OF MAILING/TRANSMISSION**

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Karen A. Hoff
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Date: 10/16/06 KAREN A. HOPF

**APPEAL BRIEF**

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicant submits the following Appeal Brief for consideration by the Board of Appeals.

## I. Real Party in Interest

The real party in interest in this matter is Ford Global Technologies, LLC, which is a wholly owned subsidiary of Ford Motor Company both in Dearborn, Michigan (hereinafter "Ford").

## II. Related Appeals and Interferences

There are no other known appeals or interferences which will directly affect or be directly affected by or have bearing on the Board's decision in the pending appeal.

## III. Status of the Claims

Claims 1-24 are pending in the application. Claims 1-24 stand rejected. The rejection of each claim is being appealed.

## IV. Status of Amendments

There have been no Amendments filed after the final rejection.

## V. Summary of Claimed Subject Matter

Claims 1, 11 and 19 are the independent claims in the case. These claims can best be understood with reference to paragraphs 17-21, and by reference to Figures 1 and 2.

Claim 1 is directed to a method for managing electrical schematic data comprising creating a logical schematic, a layout schematic, and a physical schematic for a part. Claim 1 further recites associating the logical schematic, the layout schematic, and the physical schematic together to form a part master file. The part master file is stored on a computer network. Claim 1 further recites providing access to the part master file to multiple user locations and controlling modification of the part master file so that only one of the user locations is allowed to modify the part master file at a time.

In paragraph 17 of the specification, the Applicants have specifically and explicitly defined what is meant and referred to by the terms "logical schematic", "layout schematic", and "physical schematic." The term "logical schematic" is defined as a schematic diagram comprising the logical layout of the electrical system that it describes. The logical layout is one that fully describes the electrical relationship of the circuit, but does not necessarily describe the electrical components used or the physical positioning of those components. The term "layout schematic" is defined as a schematic diagram that shows the electrical components used in the

design and the connections between them, i.e., the layout, but does not describe the exact physical positioning of the components. The "physical schematic" is defined as a schematic diagram that fully describes the electrical components used and their connections, showing the exact physical positioning of the components.

Claim 11 is directed to a system for managing electrical schematic data. Like claim 1, claim 11 also includes forming a part master file that associates the logical schematic, layout schematic and physical schematic together. Claim 11 requires the use of a computer aided engineering software program and for a computer schematic management utility which controls the modification of the part master file.

Claim 19 is directed to a method that creates a physical schematic in a single file that includes the logical schematic, layout schematic and physical schematic. Access to the part master file is provided to a plurality of user locations but only one of the user locations can modify that file.

The present invention is highly advantageous particularly as to the storing and managing electrical schematics of a product or part of a product. Each of the thousands of electrical systems of a vehicle or automobile, for example, is designed separately and often by different individuals or groups. Yet all of the parts must be compatible and must fit and work together in order to create a well designed final product. For example, all of the electrical systems of a vehicle, whether interior lighting, exterior lighting, sensors, powered accessories and the like are all interconnected to the main power distribution system of the vehicle and then to each other. With the present invention, all of the separate groups can have access to the entire master file. All have notice of all of the modifications of each component part, but only one group or user can make modifications to it at any single time.

## VI. Grounds of Rejection to be Reviewed on Appeal

The following issues are present in this appeal:

1. Are Claims 1, 3-6, 8-12, 14-19 and 21-24 properly rejected under 35 U.S.C. §102(e) as being anticipated by the Heile et al. patent (U.S. No. 6,289,319)?

2. Is Claim 7 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Heile et al. in view of VanHuben et al. (U.S. No. 6,094,654)?

3. Are Claims 3 [-sic 2], 13 and 20 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Heile et al. in view of Tou et al.?

## VII. Argument

### A. Claims 1, 3-6, 8-12, 14-19 and 21-24 are not properly rejected under 35 U.S.C. §102(e) as being anticipated by Heile et al.

Independent claims 1, 11 and 19 are all directed to methods or systems for managing electrical schematic data, the method or system having logical, layout and physical schematics for a part or component. A part master file is created and access is provided to a plurality of users. Only one user is allowed to modify the master part file at any one time.

The Heile et al. reference ("Heile") does not disclose or suggest the invention as set forth in these claims. Although Heile et al. may disclose a logical schematic, it fails to show, teach, or suggest a layout schematic and a physical schematic as defined by the present claims. Heile discloses the use of a high level block diagram of a design methodology that is used to develop a design for a programmable logic device (PLD). The blocks in the block diagram are non-implemented or un-finished and are used to create templates, which are starting points for the actual design. The high level block diagram is used prior to the creation of a logical schematic of the electrical system or the PLD. Upon creation of the templates, the system of Heile takes the source or root file of the high level block diagram and performs a simulation. In the simulation, a block functionality is reviewed by a designer. Once the results of the simulation are satisfactory, the entire design or block diagram is simulated, in which case the entire block diagram is compiled. In compilation, the language for the blocks is converted to perform a simulation. The final layout or overall design, an example of which is shown and described with respect to Figure 18 of Heile, has the gates or logic devices and the layout thereof that represent the logic of that design. The logic devices are not the actual electrical hardware components, but rather represent the logic for the hardware components.

Throughout Heile, the generation of the overall design is described. Although in Col. 22, lines 42-46, Heile discloses that the overall design may be mapped, such that the logic gates are grouped, each group corresponds to a physical device that is to perform the functions of that group. The groupings are merely hyphened blockings of the logic gates. The groupings do not show the electrical components used in the design and the connections between them or the exact physical positioning of those components, as required by the definitions of the claim terms as set forth in the specification.

Heile only shows a high-level block diagram layout, and does not show or disclose a physical schematic. However or whatever the high level block diagram and the finalized logical layout or design of Heile are referred to, the stated diagram and design are not the same as the

layout schematic and physical schematic included as components of the present claims. Thus, regardless of whether Heile links the high level block diagram and finalized logical layout or design into a master file or project file, Heile fails to teach or suggest two of the three claimed schematics and the linking thereof.

The Final Office Action asserted that Heile is directed to a compilation process for a traditional integrated circuit design, but does not address the association or lack thereof between any of the logical, layout, or physical schematics. Applicants admit that Heile is directed to the compilation process of a traditional integrated circuit design. However, the stated process only provides a logical schematic or design. The layout and physical schematics that may be associated with that design are not addressed in Heile because they are not part of the compilation process. Heile does not disclose or speak to layout and physical schematics and as such fails to teach or suggest a majority of the claimed limitations.

As such, the Heile reference fails to teach or suggest the formation of a part master file from a logical schematic, a layout schematic, and a physical schematic as recited in independent claims 1, 11, and 19 and the rejections of those claims should be reversed. The Applicants also maintain that since claims 3-6, 8-10, 12, 14-18, and 21-24 depend from their respective independent claims, they are also believed to be allowable and not properly rejected for at least the same reasons as the three independent claims.

### B. Claim 7 is not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Heile et al. in view of Van Huben et al.

Claim 7 is a dependent claim and adds to Claim 1 the additional step of storing a pointer in the part master file so that the storage location of the local, layout and physical schematics could be more readily found. Although Van Huben et al. discloses a pointer that indicates a storage location of data, that reference does not teach or suggest the step of storing a pointer in a part master file wherein the pointer indicates a storage location of a logical schematic, a physical schematic, and a layout schematic. In fact, like the Heile reference, there is no teaching or suggestion in the Van Huben reference for associating the three types of schematics, logical, layout, and physical together in one file. Thus, the rejection of claim 7 should be reversed.

### C. Claims 3 [sic 2], 13 and 20 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Heile et al. in view of Tou et al.

Claims 3, 13 and 20 were rejected under § 103(a) as being unpatentable over Heile in view of Tou et al. (Knowledge-Based Approach for the Verification of CAD Database Generated by an Automatic Schematic Capture System). First, since claim 3 [sic 2] depends from claim 1, it is novel, patentable and allowable for at least the same reasons as claim 1.

With respect to claims 13 and 20, the Examiner indicated that Heile fails to teach using a logical schematic, a layout schematic, and a physical schematic to form a schematic image file. Also, Tou et al. does not teach the creation of a part master file from a logical schematic, layout schematic and physical schematic. In fact, Tou et al. is not directed to the creation of a part master file having multiple schematics. Instead, Tou et al. is directed to the interpretation of circuit diagrams from their images. Tou et al. discloses the interpreting or processing of schematic image files into machine readable data files that CAD software can read. Simply put, Tou et al. teaches converting an image file into a readable CAD file. This is unlike the invention set forth in claims 13 and 20 which recite the inclusion of a schematic image file based on a logical schematic, a layout schematic, and a physical schematic. The conversion or translation of one file into another file is not the same as the generation of a file based on three other files. Also, the conversion of an image file into a data file is different that the generation of an image file based on three schematic files. Furthermore, claims 13 and 20 do not recite any conversion of schematics, but rather recite the formation of an image file based on schematics.

In addition, the disclosure of a CAD system, software, or files does not suggest the formation of an image file as claimed. Tou et al. discloses the conversion of image files into CAD readable data, such that they can be used for further design. The conversion of a file into a CAD format does not suggest the generation of an image file based on the schematics claimed. Thus, the rejections of claims 3 [2], 13 and 20 should be reversed.

## VIII. Claims Appendix

A copy of each of the claims involved in this appeal, namely Claims 1-24 is attached as a Claims Appendix.

## IX. Evidence Appendix

None.

## X. Related Proceedings Appendix

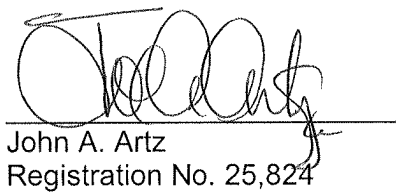
None.

## XI. Conclusion

For the foregoing reasons, Appellants respectfully request that the Board direct the Examiner in charge of this examination to withdraw the rejections of all of the claims.

Please charge any fees required in the filing of this appeal to deposit account 06-1510.

Respectfully submitted,



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## CLAIMS APPENDIX

1. A method for managing electrical schematic data comprising:

creating a logical schematic for a part;

creating a layout schematic for said part;

creating a physical schematic for said part;

associating said logical schematic, said layout schematic and said physical schematic together to form a part master file;

storing said part master file on a computer network;

providing access to said part master file to a plurality of user locations; and

controlling modification of said part master file, whereby said controlling comprises allowing only one of said plurality of user locations to modify said part master file at a time.

2. The method of claim 1, wherein said part master file further comprises a schematic image file based on said logical schematic, said layout schematic, and said physical schematic.

3. The method of claim 1, further comprising the steps of modifying said part master file and tracking a modification to said part master file.

4. The method of claim 3, wherein said tracking comprises storing a revised part master file.

5. The method of claim 3, further comprising the step of notifying an interested user location of said modifying.

6. The method of claim 1, wherein said plurality of user locations comprises at least one remote user location.

7. The method of claim 1, further comprising the step of storing a pointer in said part master file, said pointer being capable of indicating a storage location of said logical schematic, said physical schematic and said layout schematic.

8. The method of claim 1, wherein said associating is accomplished by a computer software program.

9. The method of claim 1, further comprising the steps of creating a second logical schematic for a sub-part, creating a second physical schematic for said sub-part, creating a second layout schematic for said sub-part, associating said second logical schematic, said second physical schematic and said second layout schematic together to form a sub-part master file, and storing said sub-part master file in said part master file.

10. The method of claim 9, further comprising the step of controlling modification of said sub-part master file, allowing only one of said plurality of user locations to modify said sub-part master file at a time.

11. A system for managing electrical schematic data comprising:

a computer;

at least one computer aided engineering (CAE) software program, said at least one CAE software program being capable of creating a logical schematic, a layout schematic, and a physical schematic for a part based on an input into said computer from a user;

a computer schematic management utility, said computer schematic management utility being capable of associating said logical schematic, said layout schematic and said physical schematic together to form a part master file; and

a computer network, said computer network comprising said computer and a plurality of user locations, said computer network being capable of storing said part master file and providing access to said part master file to said plurality of user locations;

whereby said computer schematic management utility controls modification of said part master file stored on said computer network.

12. The system of claim 11, wherein said computer schematic management utility controls modification of said part master file by allowing only one of said plurality of user locations to modify said part master file at a time.

13. The system of claim 11, wherein said part master file further comprises a schematic image file based on said logical schematic, said physical schematic, and said layout schematic.

14. The system of claim 11, wherein said computer schematic management utility is further capable of tracking a modification of said part master file.

15. The system of claim 14, wherein said tracking comprises storing a revised part master file.

16. The system of claim 11, further comprising an interested user list, wherein said computer schematic management utility generates a notification to said interested user list when said part master file is modified.

17. The system of claim 16, wherein said notification comprises an electronic message.

18. The system of claim 11, wherein said plurality of user locations comprises at least one remote user location.

19. A method for managing electrical schematic data comprising:

creating a logical schematic for a part with a first computer aided design tool;

creating a layout schematic for said part based on said logical schematic with a second computer aided design tool;

creating a physical schematic for said part based on said logical schematic and said layout schematic with a third computer aided design tool;

associating said logical schematic, said layout schematic and said physical schematic together to form a part master file, said associating comprising storing said logical schematic, said layout schematic, and said physical schematic in a single file;

storing said part master file on a computer network;

providing access to said part master file to a plurality of user locations; and

controlling modification of said part master file, whereby said controlling comprises allowing only one of said plurality of user locations to modify said part master file at a time.

20. The method of claim 19, wherein said part master file further comprises a schematic image file based on said logical schematic, said layout schematic, and said physical schematic.

21. The method of claim 19, further comprising the steps of modifying said part master file and tracking a modification to said part master file.

22. The method of claim 21, wherein said tracking comprises storing a revised part master file.

23. The method of claim 21, further comprising the step of notifying an interested user location of said modifying.

24. The method of claim 19, wherein said plurality of user locations comprises at least one remote user location.

## EVIDENCE APPENDIX

None.

## RELATED PROCEEDINGS APPENDIX

None.